Chapter-I

Multilevel Converters

Q-1 Explain half bridge & full bridge topology of inverter with waveforms.

ANS. DC to AC converters are known as inverters.

↳ The function of an inverter is to change a DC input voltage to symmetric ac output voltage of desired magnitude and frequency.

↳ The output voltage waveforms of ideal inverters should be sinusoidal.

↳ Single phase inverters are classified in too topologies

- Half Bridge
- Full Bridge

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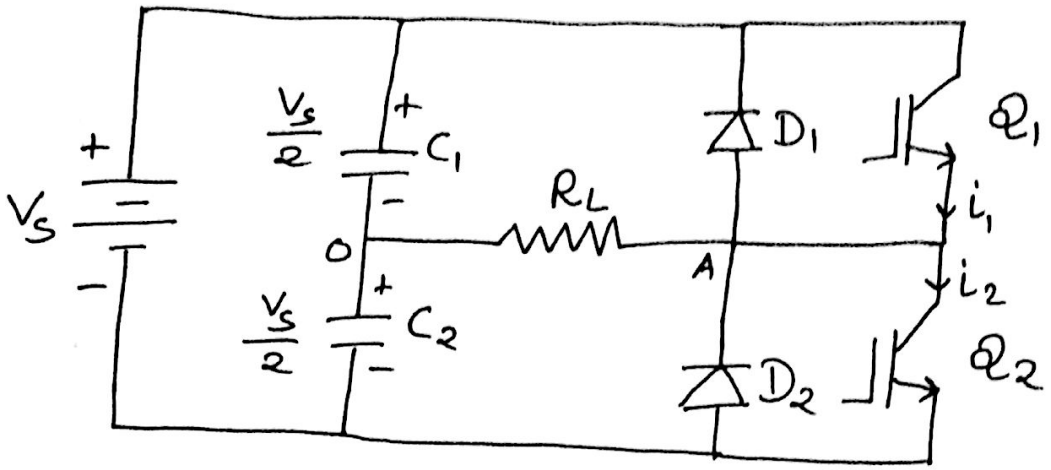
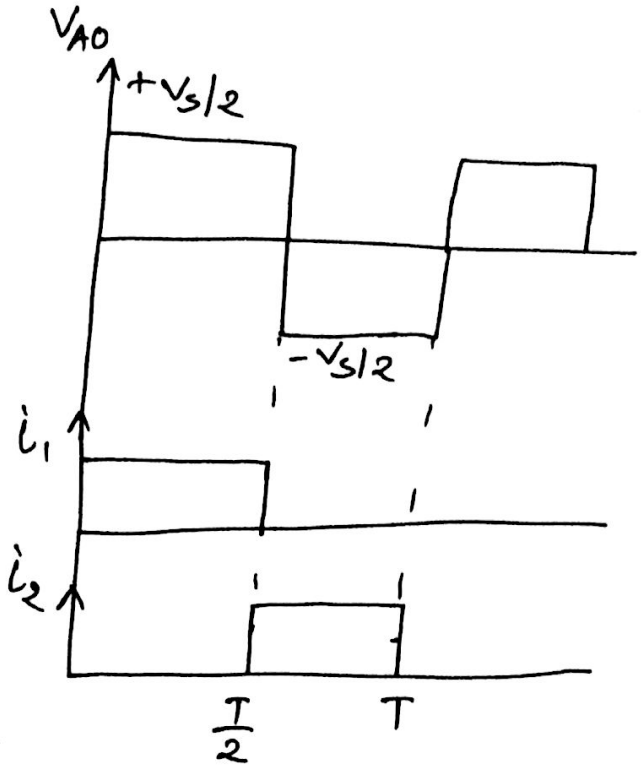
(2)

Half Bridge Inverter





↳ Inverter consists two switching Q_1 & Q_2.

↳ When Q_1 is ON for time T/2, the instantaneous voltage across the load v_o is $V_s/2$.

↳ When Q_2 is ON for a time T/2 the v_o is $-V_s/2$.

↳ The control circuit to turn ON & OFF (2)
Q_1 & Q_2 should be designed not to fire Q_1 & Q_2 at same time.

↳ The root mean square (rms) output voltage

$$V_o = \sqrt{\frac{2}{T}\int_0^{T/2} \frac{V_s^2}{4}\, dt}$$

$$= \sqrt{\frac{2V_s^2}{4T}\left[t\right]_0^{T/2}}$$

$$= \sqrt{\frac{V_s^2}{2T}\left[\frac{T}{2} - 0\right]}$$

$$= \sqrt{\frac{V_s^2}{4}}$$

$$\boxed{V_o = \frac{V_s}{2}}$$

Advantages

↳ Output voltage is half of input voltage, so when load voltage requirement is less & higher source voltage is avilebe this inverter is useful.

↳ Only two number of switches are used.

↳ Less complex control circuit.

④

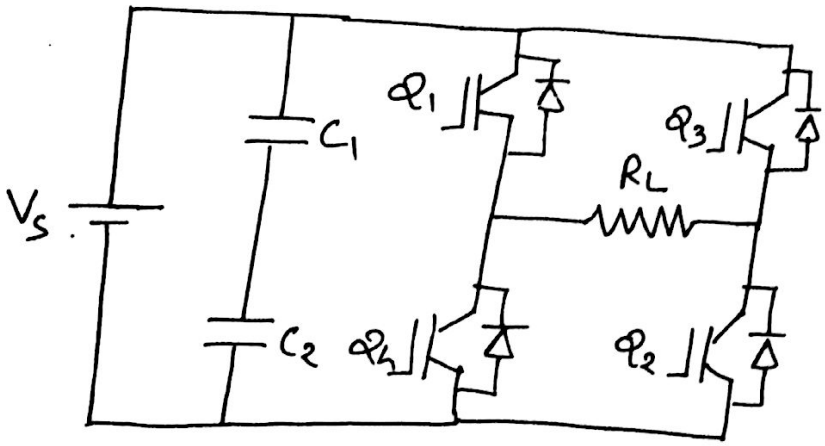
Disadvantages

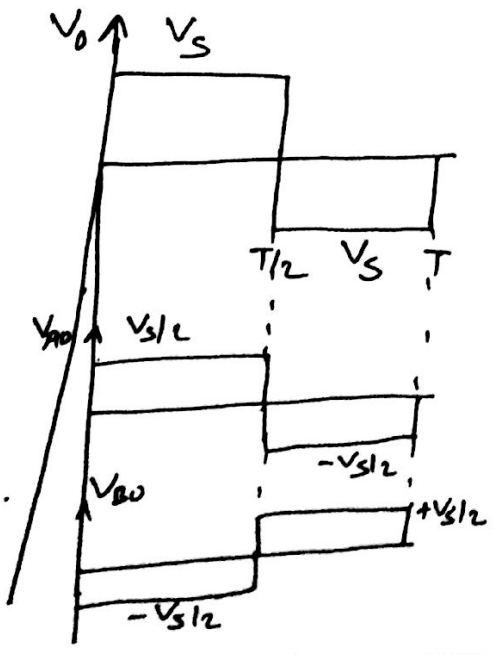
↳ It requires a 3-terminal DC source.

↳ When any one of switch is ON the other switch has to withstand entire source voltage V_s.

↳ The output of inverter is only half of input voltage.

Full Bridge Inverter





↳ This inverter consists of four switches.

↳ Q_1 & Q_2 are turned on simultaneously & the input voltage V_s appears across the load.

↳ When Q_3 & Q_4 are turned ON the voltage across the load is reversed and is $-V_s$.

↳ The rms output voltage V_o

$$V_o = \sqrt{\frac{2}{T}\int_0^{T/2} V_s^2\, dt}$$

$$= \sqrt{\frac{2V_s^2}{T}[t]_0^{T/2}}$$

$$= \sqrt{\frac{2V_s^2}{T}\left(\frac{T}{2}\right)}$$

$$\boxed{V_o = V_s}$$

Advantages

↳ RMS output voltage is V_s.

↳ Full utilization of source.

↳ Requires two terminal DC source.

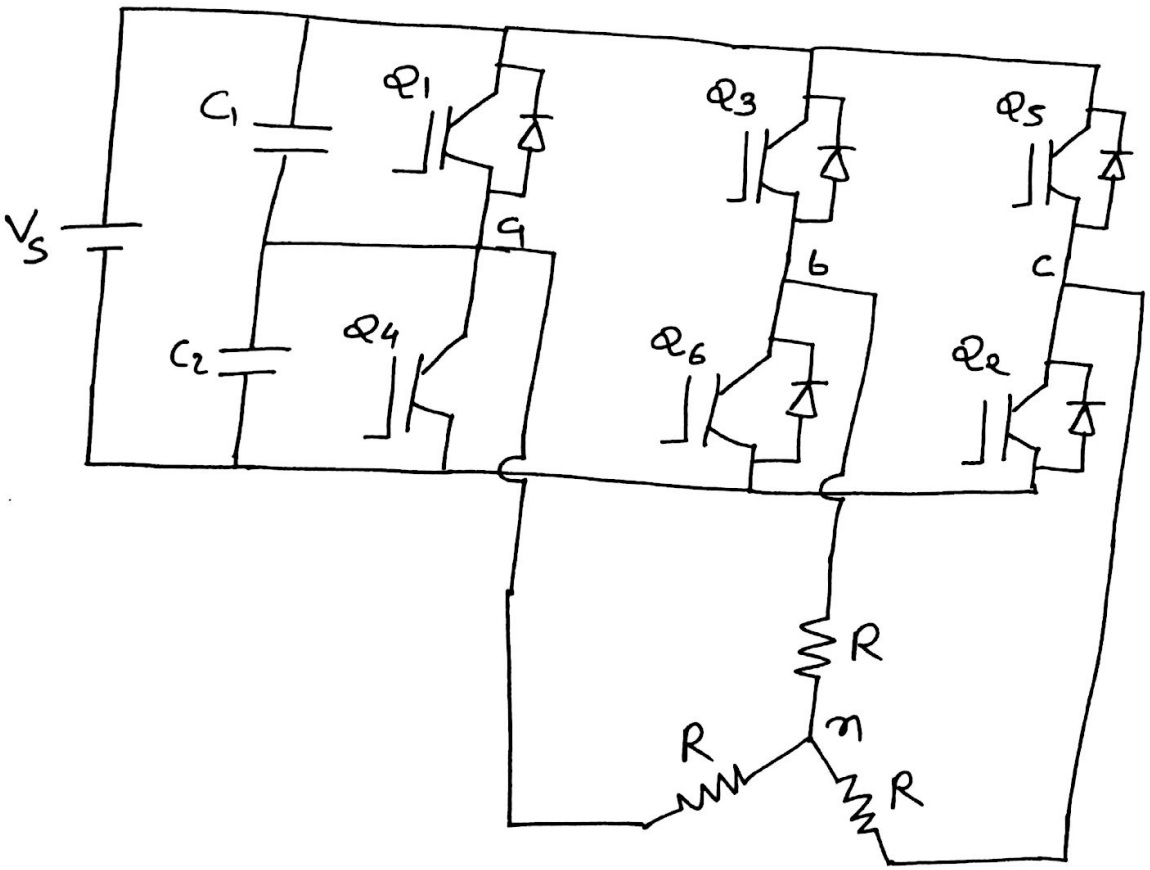
Disadvantages

↳ Four number of switches are used.

↳ complex control circuit.

Q-2 Discuss 180° conduction mode of 3-phase full bridge inverter.

ANS Three phase inverters are used for high power applications (more than 10kW).

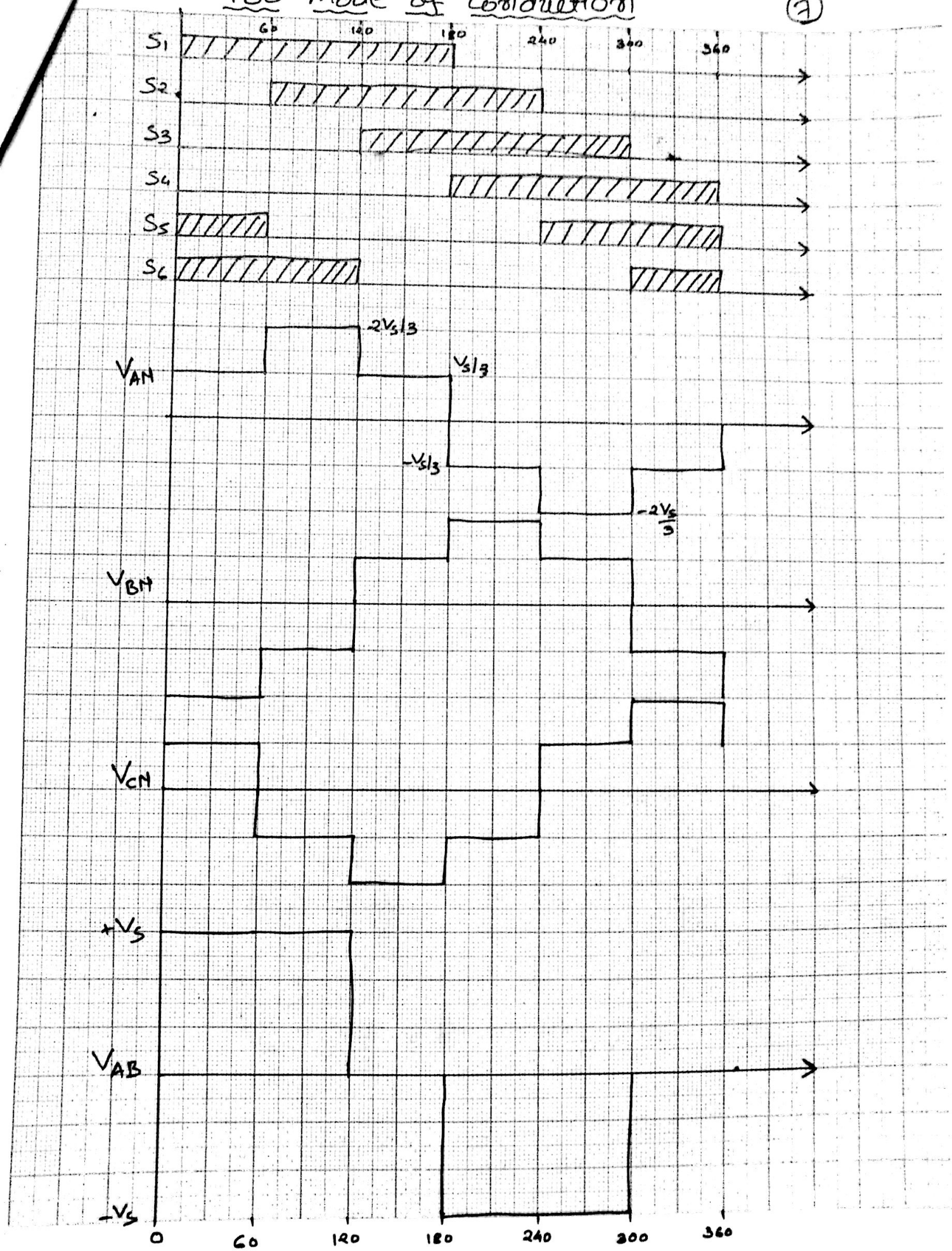


↳ In 180° conduction mode each switch conducts for 180°.

↳ At any instant of time 3 switches remain ON.

↳ When switch Q_1 is on terminal a is connected to positive terminal of the input DC source.

180° Mode of conduction



↳ When ~~terminal~~ switch Q_4 is on terminal a is connected to negative of DC source.

↳ There are six modes of operation in a cycle and duration of each mode is 60°.

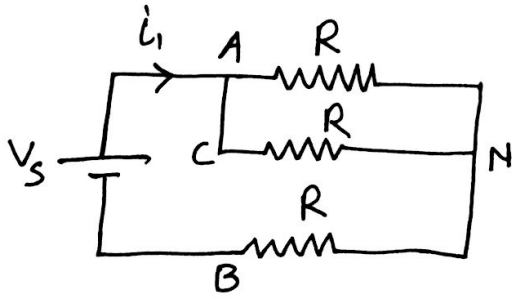
↳ The load is connected in star.

↳ switches of any leg of inverter S_1 & S_4, S_3 & S_6, S_5 & S_2 are complementry switches and can not be on simultaneously.

↳ Because it would result in short circuit across DC link voltage supply.

↳ During Mode-1 switches Q_1, Q_5 & Q_6 are ON

↳ As a result equivalent circuit



$$R_{eq} = R + \frac{R}{2} = \frac{3R}{2}$$

$$i_1 = \frac{V_s}{R_{eq}} = \frac{2V_s}{3R}$$

$$\therefore V_{AN} = \frac{i_1}{2} \times R = \frac{2V_s}{2 \times 3R} \times R = \frac{V_s}{3}$$

$$V_{BN} = -i_1 \times R = -\frac{2V_s}{3R} \times R = -\frac{2V_s}{3}$$

$$V_{CN} = \frac{i_1}{2} \times R = \frac{2V_s}{2 \times 3R} \times R = \frac{V_s}{3}$$

(9)

↳ Similarly for all mode we can find the value of phase voltages.

↳ All phase voltages at every mode is shown in the wave form.

↳ The value of line voltages can be find by $V_{AB} = V_{AN} - V_{BN}$

for mode-I

$$V_{AN} = \frac{V_s}{3}$$

$$V_{BN} = -\frac{2V_s}{3}$$

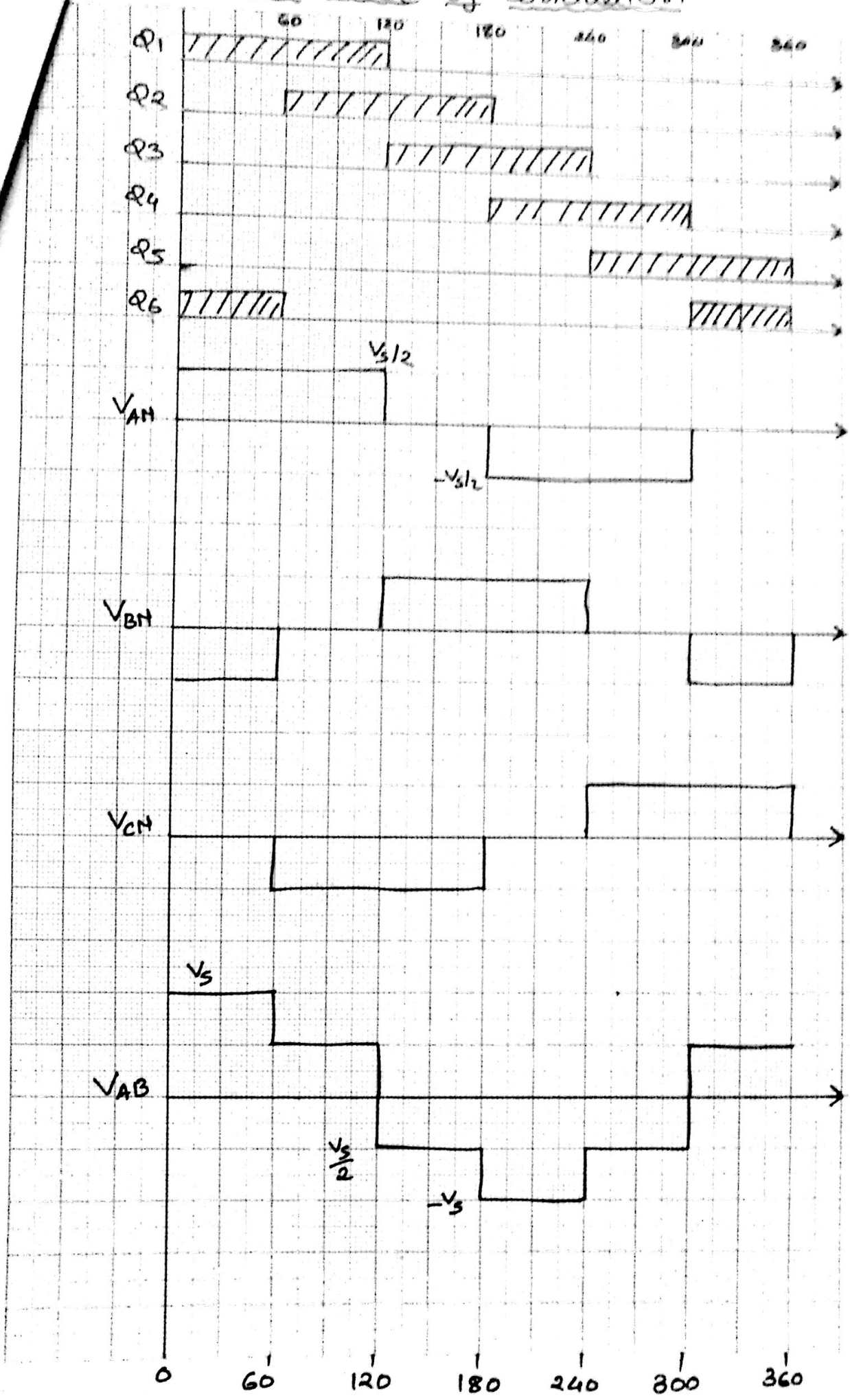
$$V_{AB} = V_{AN} - V_{BN}$$

$$= \frac{V_s}{3} - \left(-\frac{2V_s}{3}\right)$$

$$= \frac{V_s}{3} + \frac{2V_s}{3}$$

$$\underline{V_{AB} = V_s}$$

120° Mode of conduction



Q-3 Discuss 120° mode of conduction of 3-phase inverter.

ANS. Power circuit for 120° conduction & 180° conduction is same.

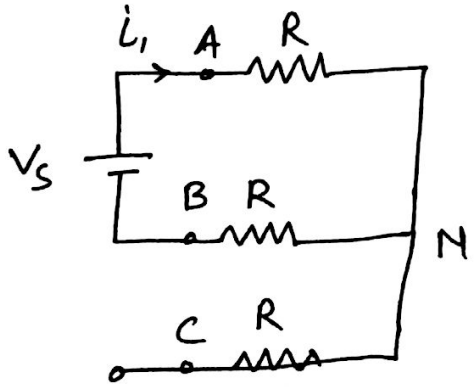
↳ The each switch conducts for 120° so the name is 120° conduction mode.

↳ In this configuration at a time only two switches are on.

↳ ~~Each switch~~ Interval between two adjacent switches is 60°.

↳ During mode-I switches Q_1 & Q_6 are ON.

↳ The equivalent circuit during mode-I



$$i = \frac{V_s}{2R}$$

$$V_{AN} = i \times R = \frac{V_s}{2R} \times R = \frac{V_s}{2}$$

$$V_{BN} = -i \times R = \frac{-V_s}{2R} \times R = \frac{-V_s}{2}$$

$$V_{CN} = 0$$

$$V_{AB} = V_{AN} - V_{BN}$$

$$= \frac{V_s}{2} - \left(\frac{-V_s}{2}\right)$$

$V_{AB} = V_s$ As shown in waveform.

(12)

Q-4 What are the features of Multilevel Inverters? Explain each in detail.

ANS. Two level inverter produce square wave output voltage waveform which contains harmonics.

↳ Multilevel inverters produce quasi-sine wave or nearly sine wave voltage output.

↳ Multilevel inverter generates the o/p voltage waveforms with more steps of smaller magnitude.

↳ It is possible to use low voltage rating power semiconductor device for multilevel inverter due to small voltage steps of o/p voltage.

↳ In multilevel inverter it is possible to obtain refined output voltage waveforms with increased number of voltage level & reduced THD in voltage.

↳ It is possible to obtain machine currents with reduced harmonics, resulting into reduced torque pulsation in the drive system.

↳ By reducing magnitude of each voltage step with increment in number of level it is possible to reduce dv/dt.

↳ By reduction in dv/dt, voltage stress on insulation is less.

↳ With lower switching frequency of operation electromagnetic interference (EMI) is reduced.

↳ Lower magnitude of common mode voltage (CMV) and in motor drive low value of bearing current flows.

↳ As switching frequency is reduced the switching losses are also very less.

Q-5 classify multilevel inverter and write down the applications of multilevel inverters. Q-6

ANS. The multilevel inverters are classified in major three categories as follows.

↳ Neutral point clamped (Diode clamped)

↳ Flying capacitor

↳ H- Bridge inverter
- Symmetrical H-Bridge
- Asymmetrical H-Bridge

Applications of Multilevel Inverters.

↳ High power, high voltage adjustable speed drives (ASD)
↳ Laminators
↳ Rolling mills
↳ Conveyors
↳ Compressors
↳ Pumps
↳ Fans
↳ Marine
↳ Blowers

(Diode clamped)

Q-6 Explain Neutral Point clamped 3-level inverter with switching table, circuit diagram and relevent waveforms. (15)

ANS. In this topology of multilevel inverter the DC link is split into number of small voltage levels using a bank of series connected bulk-capacitors.

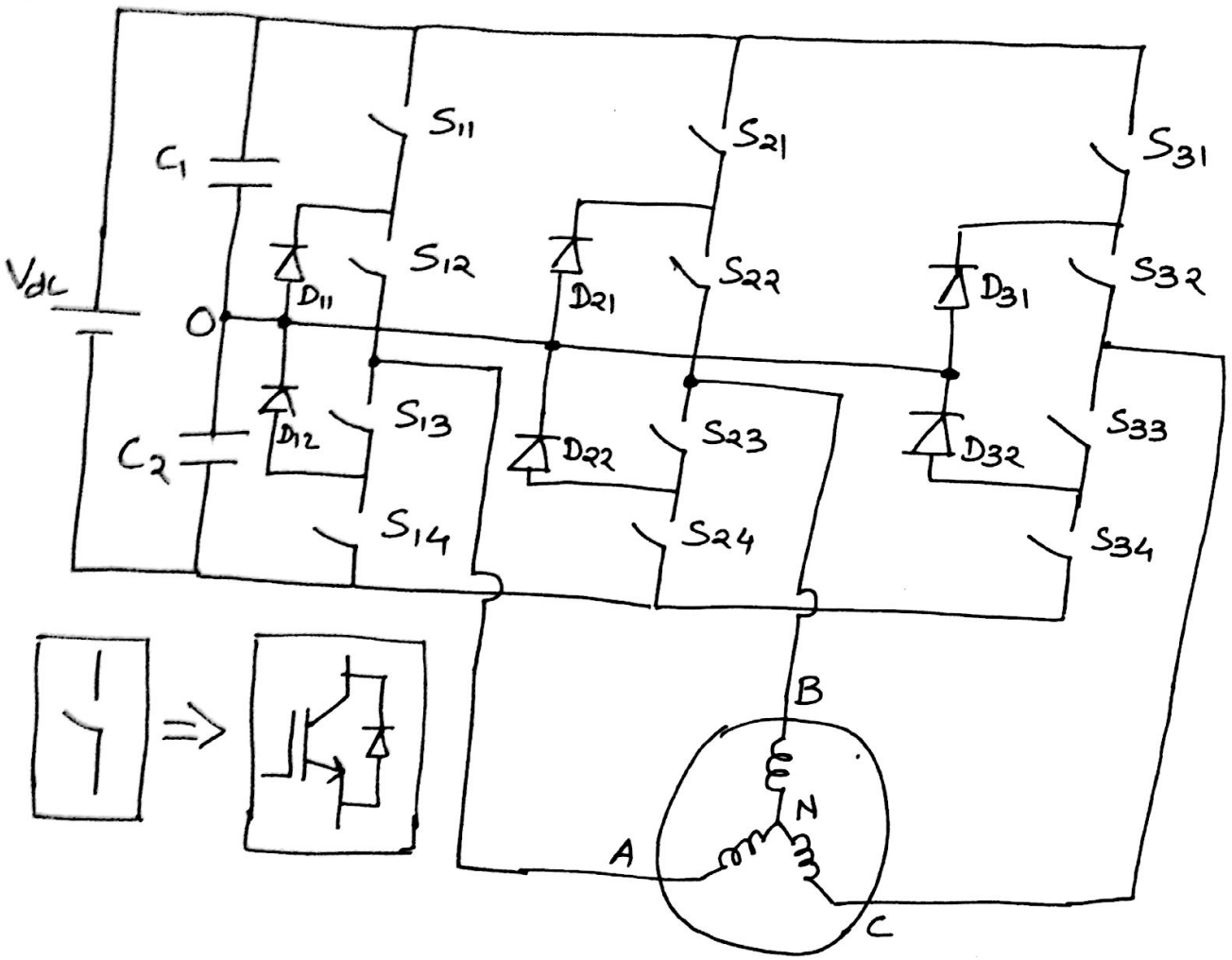
↳ The inverter structure allows the connections of the inverter poles to any one of these voltage levels thus generating a multi-level voltage waveform.

↳ In this inverter topology middle point O of the two DC link capacitors C_1 & C_2 is defined as a Neutral point.

↳ Here as the mid voltage level is formed by clamping the switching devices to the neutral-point of the DC-bus.

↳ Each leg of the inverter consists of four switches and two diodes (clamping diodes).

(16)



Pole voltage V_{AO}	S_{11}	S_{12}	S_{13}	S_{14}
$+\frac{V_{DC}}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{V_{DC}}{2}$	0	0	1	1

S_{11} & S_{13} } complementry
S_{12} & S_{14} }

1 => ON state

0 => OFF state

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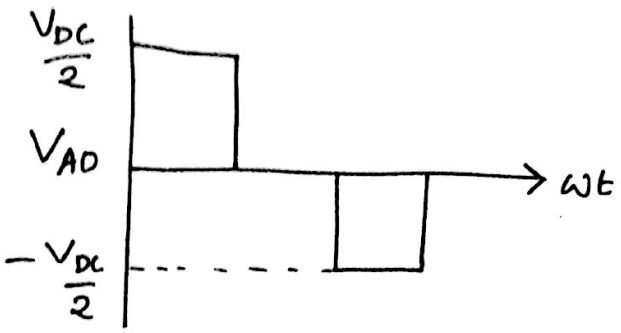


Pole voltage V_{AO}

↳ Each pole of this inverter can attain one of the three voltage levels

$$+\frac{V_{DC}}{2}, \quad 0 \quad \& \quad -\frac{V_{DC}}{2}$$

with respect to neutral point O.

↳ Pole voltage V_{AO} attains the level of $V_{DC}/2$ when top switches S_{11} & S_{12} are ON.

↳ Level $-V_{DC}/2$ is realized when the bottom switches S_{13} & S_{14} are turned ON.

↳ Zero voltage level is obtained when inner two switches S_{12} & S_{13} are turned ON and the V_{AO} gets clamped to the neutral point through Diodes D_{11} & D_{12} depending on the direction of the load current.

Q-7 Discuss 3-level flying capacitor inverter topology in detail.

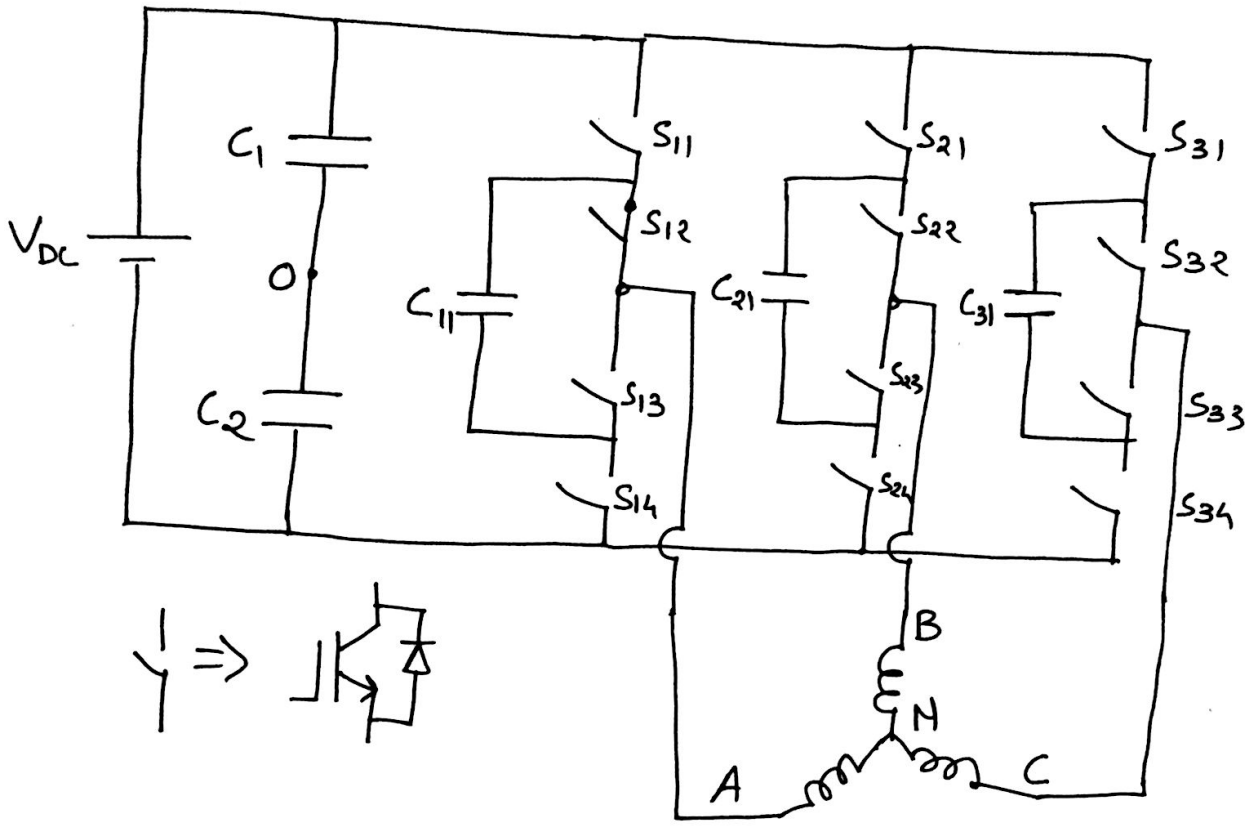
ANS. In this topology of multilevel inverter there is a one capacitor which acts as a floting source of energy charge to $\frac{V_{DC}}{2}$.

↳ This circuit is called flying capacitor (capacitor clamped) multilevel inverter.

↳ As independent capacitor clamp the device voltage to one capacitor voltage level.

↳ In this configuration the capacitor can be kept charged to half the DC-link voltage and the capacitor voltage can be added or subtracted from the DC-link voltage to generate more levels at the output pole of the inverter.

↳ Inverter consists of four switches and a capacitor connected between inner two switches as shown in circuit diagram.



Pole voltage V_{AO}	S_{11}	S_{12}	S_{13}	S_{14}	C_{11}
$V_{DC}/2$	1	1	0	0	No effect
Zero level	1	0	1	0	charging
	0	1	0	1	Discharging
$-V_{DC}/2$	0	0	1	1	No effect

S_{11} & S_{14} } Complementry Pair of switches
S_{12} & S_{13} }

1 $\Rightarrow$ ON state

0 $\Rightarrow$ OFF state

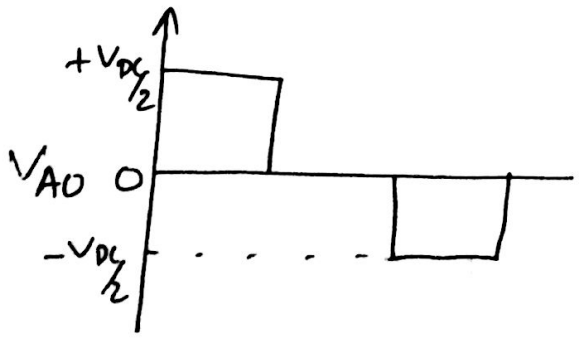
↳ When switches S_{11} & S_{12} are ON, the output pole voltage V_{AO} is $+V_{DC}/2$.

↳ Pole voltage level $-V_{DC}/2$ is obtain when bottom switches S_{13} & S_{14} are turned ON.

↳ Zero voltage level can be attain by two switching states.

↳ S_{11} & S_{13} are turned ON capacitor C_{11} is charging and $+\frac{V_{DC}}{2}$ voltage is subtracted from the DC-link voltage which is $V_{DC}/2$ and hence zero voltage level appears.

↳ switches S_{12} & S_{14} are turned ON and capacitor C_{11} is discharging and voltage $-\frac{V_{DC}}{2}$ is added to the DC-link voltage $V_{DC}/2$ and zero voltage level is attained.



Pole voltage

V_{AO}

Q-8 Explain the DC voltage balance techniques for capacitor clamped multilevel inverters.

ANS. Flying capacitor topology has two different switching state for zero voltage level.

↳ This is called redundancy.

↳ The availability of voltage redundancies allows controlling the individual capacitor voltages.

↳ To produce the same output voltage, the inverter has different combinations of capacitor charging or discharging.

↳ This flexibility makes it easier to manipulate the capacitor voltages and keep them at their proper values.

↳ It is possible to make individual capacitor to charge or discharge by selection of proper switching state.

↳ Thus by proper selection of switching capacitor voltage can be balanced.

Q-9 Explain different H-bridge topology of multilevel inverter. Write down advantages and disadvantages of the H-bridge topology over other inverter topology.

ANS. H-Bridge inverter topology is the most Popular converter topologies used in high-power medium voltage drives.

↳ It is composed of a multiple units of single phase H-bridge power cells.

↳ The H-bridge cells are normally connected in cascade on their ac side to achive medium-voltage operation and low harmonic distortion.

↳ This topology requires a number of isolated DC supplies each of which feeds an H-bridge power cell.

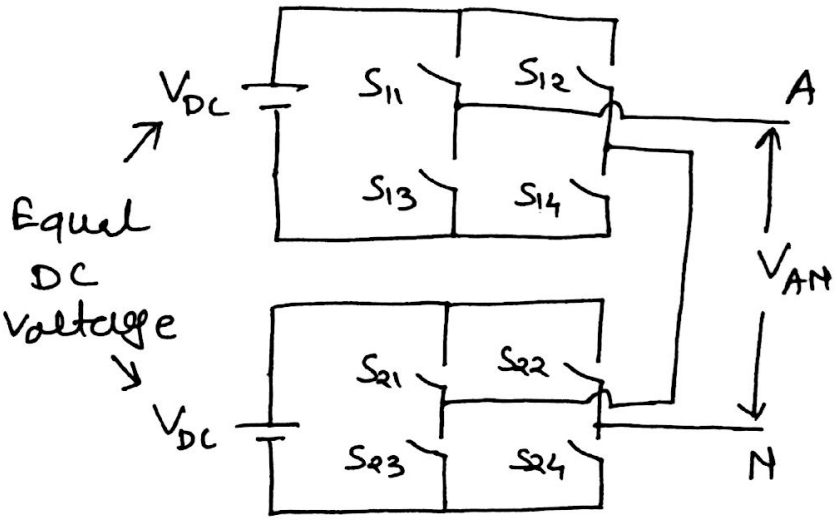
↳ There are mainly two H-bridge topology are there.

↳ Symmetric topology

↳ Asymmetric topology

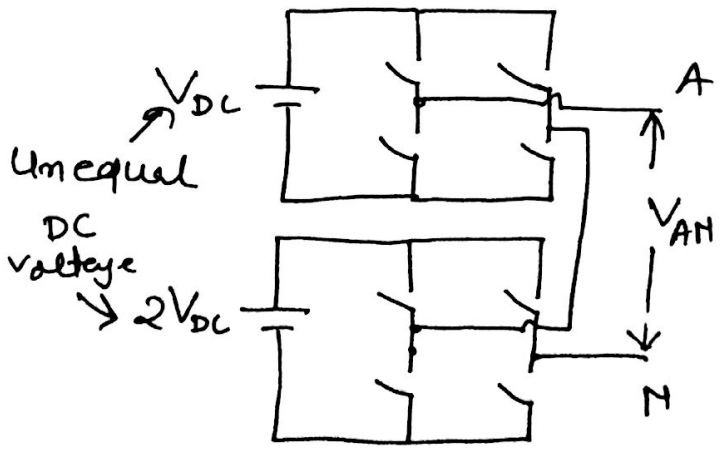
↳ Symmetric

↳ In symmetric topology each power cell is powered by an isolated DC supply of equal voltage. V_{DC}



↳ Asymmetric

↳ Asymmetric topology consists of unequal voltage of isolated DC supply to power each power cell.



Advantages

↳ Modular structure:-

This topology is composed of multiple units of identical H-bridge power cells, which leades to reduction in manufacturing cost.

↳ Low THD:-

The inverter voltage waveform is formed by a several voltage levels with small voltage steps, so inverter o/p voltage waveform is very near to a sine wave.

↳ Low dv/dt:-

As small ~~number~~ of voltage steps forms inverter o/p voltage, dv/dt is very less compared to other inverter topology.

↳ High-voltage operation without switching device in series:

More number of power cell compose high inverter output voltage.

Disadvantages

↳ Large number of dc supplies:-

Each power cell requires a isolated DC power supply.

↳ Large number of switches are required.